HELIOS

pHotonics ELectronics functional Integration on CMOS

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Basic information about HELIOS

- Large-scale integrating project (IP)
- Start date: 1 May 2008
- Duration: 48 months
- Total budget: 12.048 M€
- Total EC funding: 8.500 M€

Rationale of the project

- Integration of photonics with electronics is needed for improving system **performance** while **reducing size and cost**
- The key for the success of integration are:
  - Generic wafer-scale integration technologies
  - Small set of elementary components
  - Use of standard design environment and process
  - Technology available through a foundry model → fabless approach

Objectives (1)

- Build a complete **design and fabrication chain** enabling the integration of a **photonic layer** with a **CMOS circuit**, using **microelectronics fabrication processes**.
- It will make accessible integration technologies for a broad circle of users in a foundry-like, fabless way

Objectives (2)

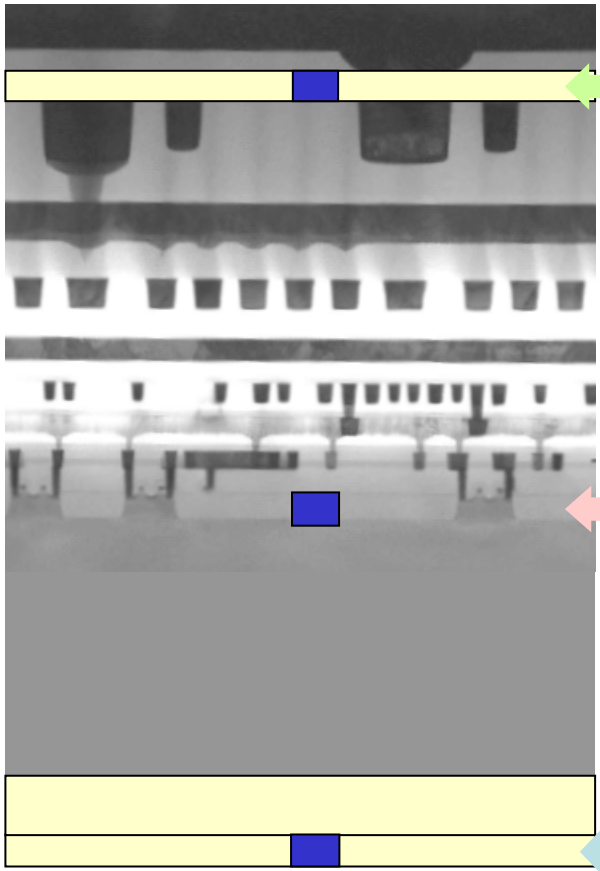
- Development of high performance generic building blocks that can be used for a broad range of applications:
  - **WDM sources by III-V/Si heterogeneous integration**
  - **Fast modulators and detectors,**
  - **Passive circuits and packaging**
- Building and optimization of the whole “food chain” to fabricate complex functional devices.
- Investigation of more promising but challenging alternative approaches for the next generation of devices
- Road mapping, dissemination and training, to strengthen the European research and industry in this field and to raise awareness of new users about the interest of CMOS Photonics.

Scientific and technological challenges (1)

- High performance building blocks:
  - Integrated III-V/Si laser 3dBm output power, single mode operation, 30dB SMSR, CW laser operation at 65°C
  - 40Gbit/s modulators array with 2 dB active modulation depth, 6dB insertion loss
  - Ge or InGaAs Photodetector BW= 30 GHz, R>0.8 A/W, Id <50mA/cm^2
- Alternative approaches:
  - use of silicon related materials as active materials
  - generic architecture (2.5D approach) for the III-V / Si heterogeneous integration of active devices on CMOS

Scientific and technological challenges (2)

Integration of complex photonic functions with EIC



Photonic layer at the last levels of metallizations with back-end fabrication

- BE fab(<400°C) or FE fab with wafer bonding
- Use of standard FE CMOS technologies
- Heterogeneous integration of III-V on Si
- High integration density (AboveIC)
- Multilevel process capability

Combined front-end fabrication

- Specific FE CMOS technology and library
- Flip-Chip hybridization of InP components
- Moderate integration density
- Efficient connections of EIC and PIC

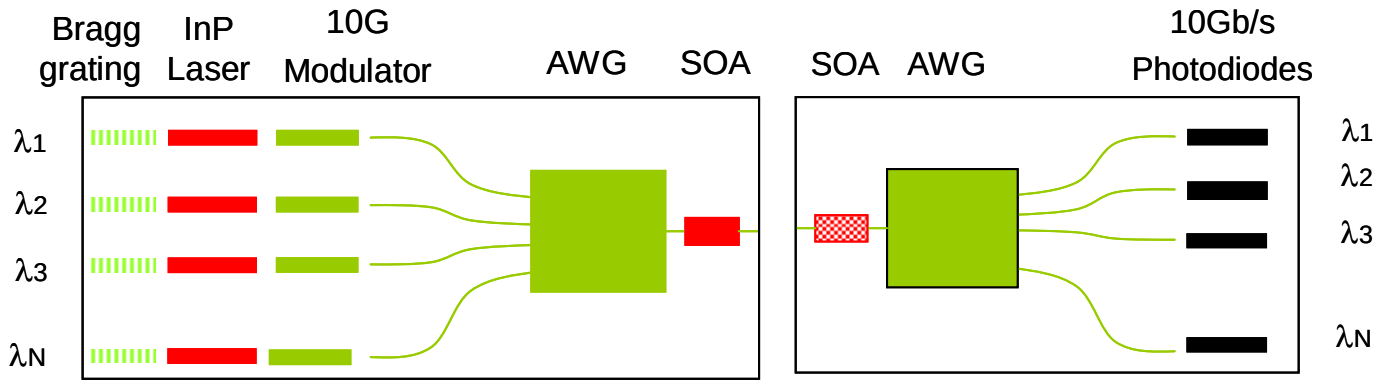
Backside fabrication

- BE fab(<400°C) or FE fab with wafer bonding
- Through substrate connections
- High integration density
- Heterogeneous integration of III-V on Si

BE: Back end FE:Front end

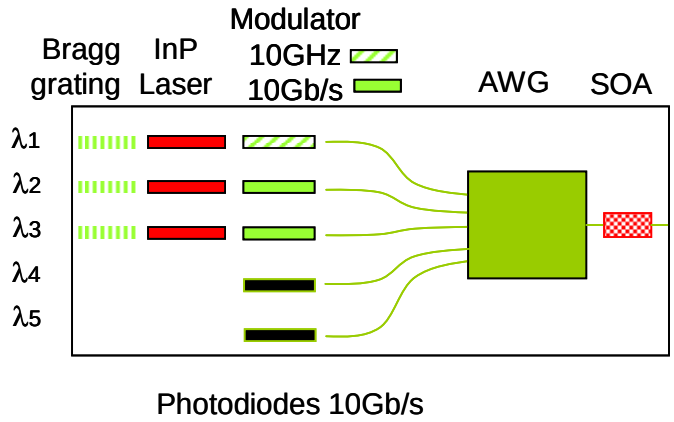
Demonstrators (1)

- 40Gb/s modulator on a EIC
  - Integration of modulator, monitoring PD and driver
- 10x10 Gb/s transceiver

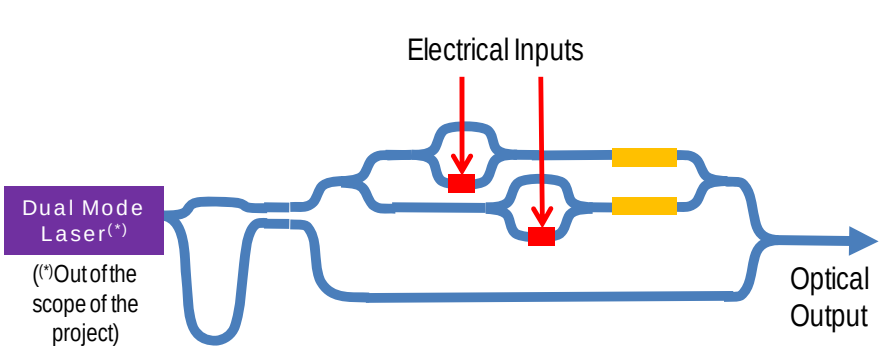


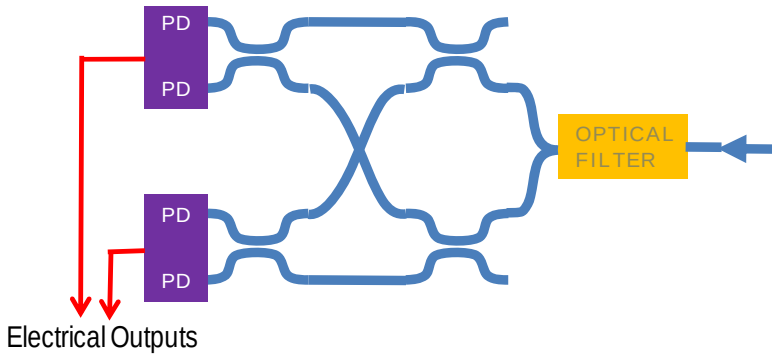
Demonstrators (2)

- Mixed analog and digital transceiver module for multifunction antennas



- Photonic QAM-10Gb/s wireless transmission system





Application domains

- The demonstrators and first applications are in the telecom/datacom field

but …

- The results of HELIOS will pave the way for applications of CMOS photonics for other fields, eg sensors, instrumentation, optical processing

Consortium

- Different but complementary skills are requested to fulfill the project objectives:
  - Industrial end-users to drive the project, define the components architecture and specifications — Photline, DAS Photonics, Thales, (Avanex)
  - III-V industrials to develop III-V on silicon approach, benchmarking — Alcatel Thales III-V lab, 3S Photonics
  - CMOS foundries and design tools experts to ensure technological relevance, photonic/electronic convergence and facilitate further exploitation — AMS, IHP, Phoenix, CNRS, TU Vienna
  - CMOS photonics institutes to develop processes and enable the transfer to foundries — LETI, IMEC
  - Academic laboratories to optimize generic building blocks and develop innovative architectures — CNRS, UNIS, IMM, UPS, UPV, UNITN, UB, TUB